Figure 3.6
Synthesizable predefined data types with corresponding package of origin and dimensionality (additions made in VHDL 2008 are inside gray areas).

Category	Package of origin	Predefined synthesizable types	Dimension
Standard	standard	BIT	Scalar
		BIT_VECTOR	1D
		BOOLEAN	Scalar
		INTEGER	1D
		NATURAL	1D
		POSITIVE	1D
		CHARACTER	1D
		STRING	1Dx1D
	standard (2008 expansion)	BOOLEAN_VECTOR	1D
		INTEGER_VECTOR	1DX1D
	numeric_bit_unsigned (2008)	(only operators for BIT and BV)	---
Standard logic	std_logic_1164	STD_(U)LOGIC	Scalar
		STD_(U)LOGIC_VECTOR	1D
	std_logic_1164 (2008 expansion)	STD_(U)LOGIC	Scalar
		STD_(U)LOGIC_VECTOR	1D
	std_logic_unsigned	(only operators for SLV)	---
	std_logic_signed	(only operators for SLV)	---
	numeric_std_unsigned (2008)	(only operators for SL and SLV)	---
Unsigned and Signed	numeric_bit	UNSIGNED (base=BIT)	1D
		SIGNED (base=BIT)	1D
	numeric_std	UNSIGNED (base=STD_LOGIC)	1D
		SIGNED (base=STD_LOGIC)	1D
	std_logic_arith	UNSIGNED (base=STD_LOGIC)	1D
		SIGNED (base=STD_LOGIC)	1D
Fixed and Floating point	fixed_pkg + associated packages (2008)	UFIXED	1D
		SFIXED	1D
	float_pkg + assoc. pack. (2008)	FLOAT	1D

Figure 4.1
Predefined operators and corresponding synthesizable predefined data types (the gray area contains the operators introduced in VHDL 2008).

Operator type	Predefined operators	Supported synthesizable predefined data types (*)
Logical	NOT, AND, NAND, OR, NOR, XOR, XNOR	BIT, BIT_VECTOR, BOOLEAN, BOOLEAN_VECTOR(1), STD_(U)LOGIC, STD_LOGIC_(U)VECTOR, (UN)SIGNED(2), UFIXED(1), SFIXED(1), FLOAT(1)
Arithmetic	+, –, *, /, **, ABS, REM, MOD	INTEGER, NATURAL, POSITIVE, STD_(U)LOGIC_VECTOR(3), (UN)SIGNED(4), UFIXED(1), SFIXED(1), FLOAT(1)
Comparison	=, /=, >, <, >=, <=	BIT, BIT_VECTOR, BOOLEAN, BOOLEAN_VECTOR(1), INTEGER, NATURAL, POSITIVE, INTEGER_VECTOR(1), CHARACTER, STRING, STD_(U)LOGIC_VECTOR(3), (UN)SIGNED(4), UFIXED(1), SFIXED(1), FLOAT(1)
Shift	SLL, SRL, SLA, SRA, ROL, ROR	BIT_VECTOR, BOOLEAN_VECTOR(1), STD_LOGIC_(U)VECTOR(3), (UN)SIGNED(4), UFIXED(1), SFIXED(1)
Concatenation	& (" , " and OTHERS too)	BIT_VECTOR, BOOLEAN_VECTOR(1), INTEGER_VECTOR(1), STRING, STD_(U)LOGIC_VECTOR, (UN)SIGNED(4)
Matching comparison (1)	?=, ?/=, ?>, ?<, ?>=, ?<=	BIT, BIT_VECTOR(*), BOOLEAN_VECTOR(*), STD_(U)LOGIC, STD_(U)LOGIC_VECTOR, (UN)SIGNED(2), UFIXED(1), SFIXED(1), FLOAT(1)
Condition (1)	??	BIT, STD_(U)LOGIC
Min/Max and String conversion (1)	MINIMUM, MAXIMUM, TO_STRING, etc.	Nearly all VHDL types in standard packages (see appendices)
(*) Note: Some types support only a partial set of operators (1) Introduced or proposed in VHDL 2008 (2) With package numeric_std		(3) Requires package std_logic_(un)signed or numeric_std_unsigned (4) Requires package numeric_std or std_logic_arith

Figure 3.10
Main type-conversion options (type casting and type-conversion functions).

From	To	Type conversion function	Package of origin
INTEGER	STD_LOGIC_VECTOR	conv_std_logic_vector(a, cs)	std_logic_arith
	UNSIGNED	to_unsigned(a, cs) conv_unsigned(a, cs)	numeric_std std_logic_arith
	SIGNED	to_signed(a, cs) conv_signed(a, cs)	numeric_std std_logic_arith
	UFIXED	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
BIT_VECTOR	STD_LOGIC_VECTOR	to_stdlogicvector(a, cs)	std_logic_1164
STD_LOGIC_VECTOR	INTEGER	conv_integer(a, cs) conv_integer(a, cs) to_integer(a, cs)	std_logic_signed std_logic_unsigned numeric_std_unsigned
	BIT_VECTOR	to_bitvector(a, cs)	std_logic_1164
	UNSIGNED	unsigned(a) (*) unsigned(a) (*)	numeric_std std_logic_arith
	SIGNED	signed(a) (*) signed(a) (*)	numeric_std std_logic_arith
	UFIXED	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
UNSIGNED and SIGNED	INTEGER	to_integer(a, cs) conv_integer(a, cs)	numeric_std std_logic_arith
	STD_LOGIC_VECTOR	std_logic_vector(a) (*) std_logic_vector(a) (*) conv_std_logic_vector(a, cs)	numeric_std std_logic_arith std_logic_arith
	UNSIGNED	conv_unsigned(a, cs)	std_logic_arith
	SIGNED	conv_signed(a, cs)	std_logic_arith
	UFIXED (unsigned only)	to_ufixed(a, cs)	fixed_generic_pkg
	SFIXED (signed only)	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
UFIXED and SFIXED	INTEGER	to_integer(a, cs)	fixed_generic_pkg
	STD_LOGIC_VECTOR	to_slv(a, cs)	fixed_generic_pkg
	UNSIGNED (ufixed only)	to_unsigned(a, cs)	fixed_generic_pkg
	SIGNED (sfixed only)	to_signed(a, cs)	fixed_generic_pkg
	SFIXED (ufixed only)	to_sfixed(a, cs)	fixed_generic_pkg
	FLOAT	to_float(a, cs)	float_generic_pkg
FLOAT	INTEGER	to_integer(a, cs)	float_generic_pkg
	STD_LOGIC_VECTOR	to_slv(a, cs)	float_generic_pkg
	UNSIGNED	to_unsigned(a, cs)	float_generic_pkg
	SIGNED	to_signed(a, cs)	float_generic_pkg
	UFIXED	to_ufixed(a, cs)	float_generic_pkg
	SFIXED	to_sfixed(a, cs)	float_generic_pkg
(a, cs) = (argument, conversion specifications) cs may include vector size, left/right range constants, overflow and rounding specs, etc. (consult package) (*) = type casting			

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