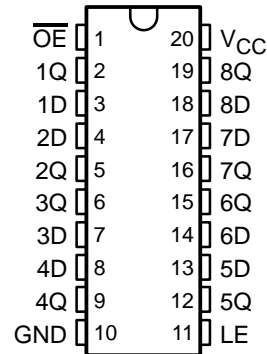


CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS452A – FEBRUARY 2001 – REVISED APRIL 2003

- 2-V to 6-V V_{CC} Operation
- Wide Operating Temperature Range of -55°C to 125°C
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive up to 15 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs

CD54HC373 . . . F PACKAGE
CD74HC373 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'HC373 devices are octal transparent D-type latches designed for 2-V to 6-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74HC373E	CD74HC373E
	SOIC – M	Tube	CD74HC373M	HC373M
		Tape and reel	CD74HC373M96	
	CDIP – F	Tube	CD54HC373F3A	CD54HC373F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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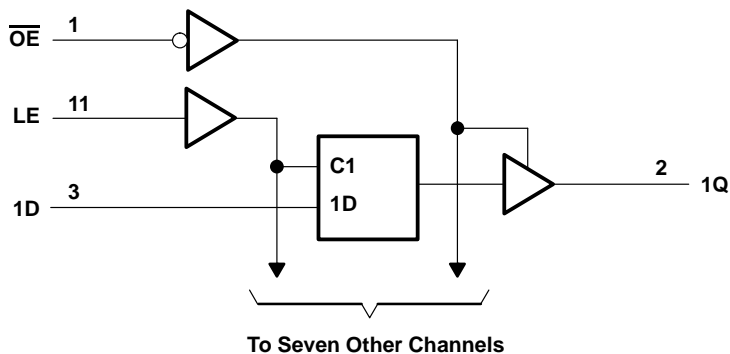
CD54HC373, CD74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	69°C/W
M package	58°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

CD54HC373, CD74HC373
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 4.5 V	3.15	
		V _{CC} = 6 V	4.2	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 4.5 V	1.35	
		V _{CC} = 6 V	1.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	1000	ns
		V _{CC} = 4.5 V	500	
		V _{CC} = 6 V	400	
T _A	Operating free-air temperature	-55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.9	1.9	V		
			4.5 V	4.4	4.4	4.4			
			6 V	5.9	5.9	5.9			
		I _{OH} = -6 mA	4.5 V	3.98	3.7	3.84			
		I _{OH} = -7.8 mA	6 V	5.48	5.2	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.1	0.1	0.1	V		
			4.5 V	0.1	0.1	0.1			
			6 V	0.1	0.1	0.1			
		I _{OL} = 6 mA	4.5 V	0.26	0.4	0.33			
		I _{OL} = 7.8 mA	6 V	0.26	0.4	0.33			
I _I	V _I = V _{CC} or 0	6 V	±0.1	±1	±1	μA			
I _{OZ}	V _O = V _{CC} or 0	6 V	±0.5	±10	±5	μA			
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V	8	160	80	μA			
C _i			10	10	10	pF			
C _o			20	20	20	pF			

CD54HC373, CD74HC373
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, LE high	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t_{su} Setup time, data before LE↓	2 V	50		75		65		ns
	4.5 V	10		15		13		
	6 V	9		13		11		
t_h Hold time, data after LE↓	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

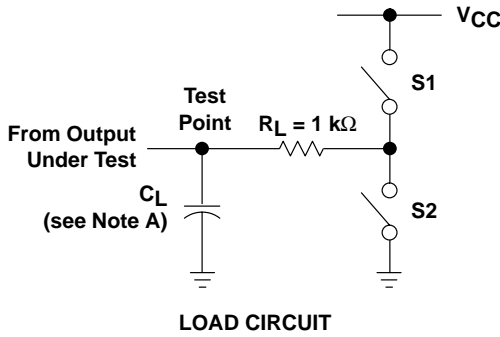
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
	LE	Q	$C_L = 50\text{ pF}$	2 V	175		265		220		
				4.5 V	35		53		44		
				6 V	30		45		37		
t_{en}	\overline{OE}	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
t_{dis}	\overline{OE}	Q	$C_L = 50\text{ pF}$	2 V	150		225		190	ns	
				4.5 V	30		45		38		
				6 V	26		38		33		
t_t		Q	$C_L = 50\text{ pF}$	2 V	60		90		75	ns	
				4.5 V	12		18		15		
				6 V	10		15		13		

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

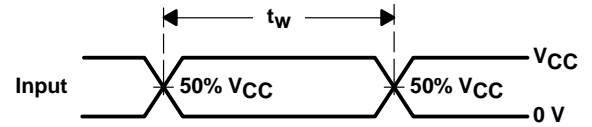
PARAMETER	TYP	UNIT
C_{pd} Power dissipation capacitance	51	pF



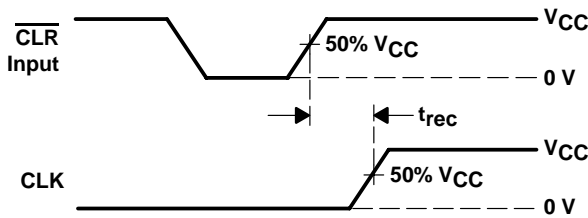
PARAMETER MEASUREMENT INFORMATION



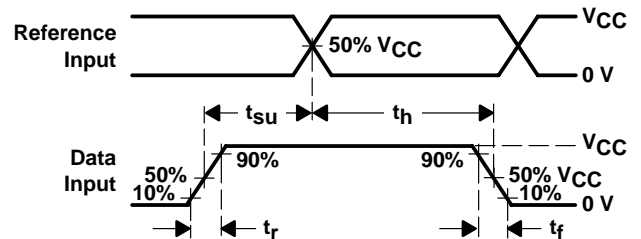
PARAMETER	S1	S2
t_{en}	tpZH	Open
	tpZL	Closed
t_{dis}	tpHZ	Open
	tpLZ	Closed
t_{pd} or t_f	Open	Open



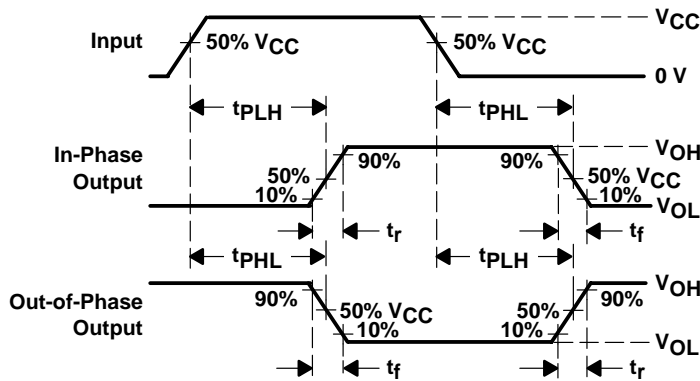
VOLTAGE WAVEFORMS
 PULSE DURATION



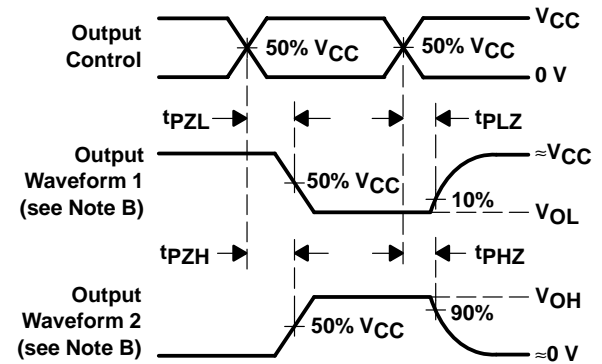
VOLTAGE WAVEFORMS
 RECOVERY TIME



VOLTAGE WAVEFORMS
 SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
 OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 G. t_{pZL} and t_{pZH} are the same as t_{en} .
 H. t_{pLH} and t_{pHL} are the same as t_{pd} .
 I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54HC373F	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54HC373F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD74HC373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC373M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HC373M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

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