

**PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M  
PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M  
STANDARD HIGH-SPEED PAL® CIRCUITS**

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

- **Choice of Operating Speeds**  
High-Speed, A Devices . . . 25 MHz Min  
Half-Power, A-2 Devices . . . 16 MHz Min
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

**description**

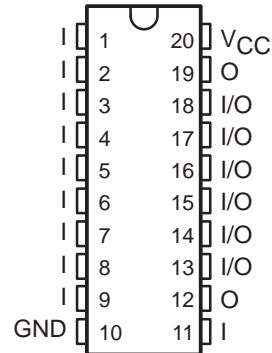
These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

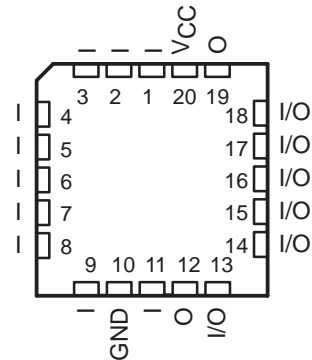
**PAL16L8'  
J OR W PACKAGE**

(TOP VIEW)



**PAL16L8'  
FK PACKAGE**

(TOP VIEW)



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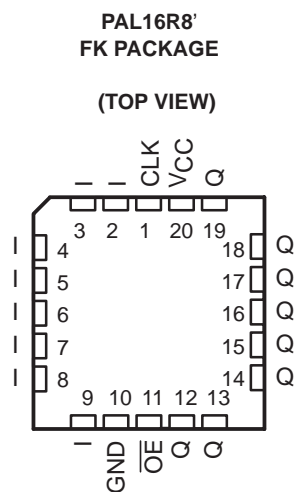
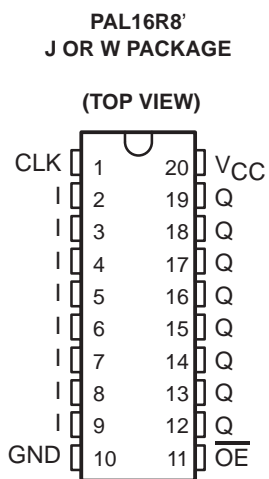
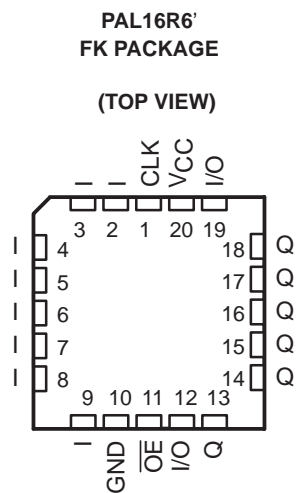
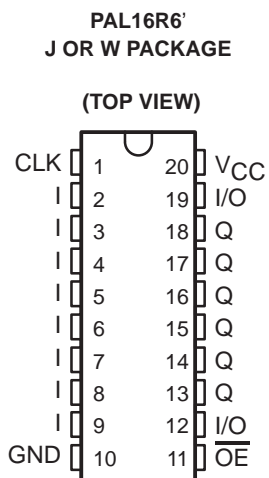
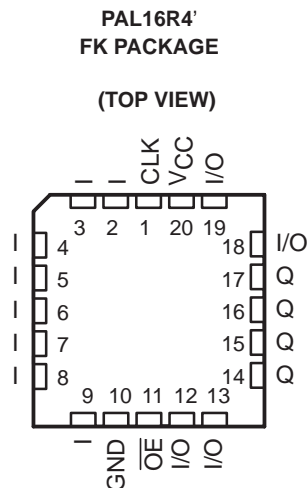
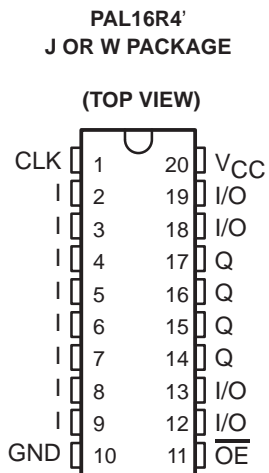


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# PAL16R4AM, PAL16R4A-2M, PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

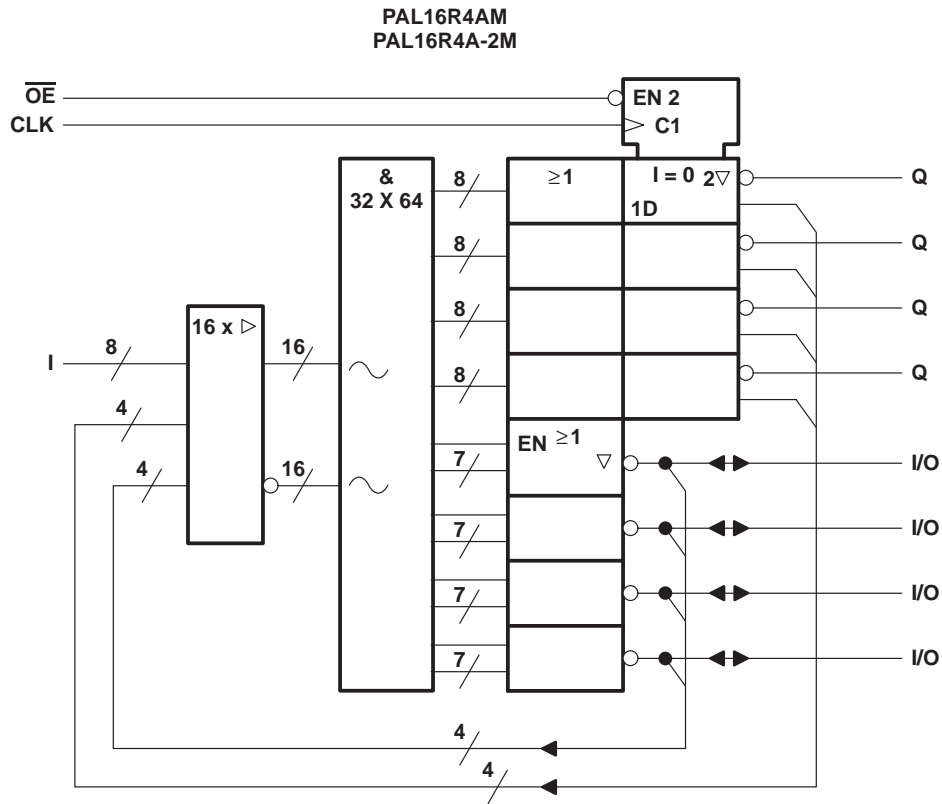
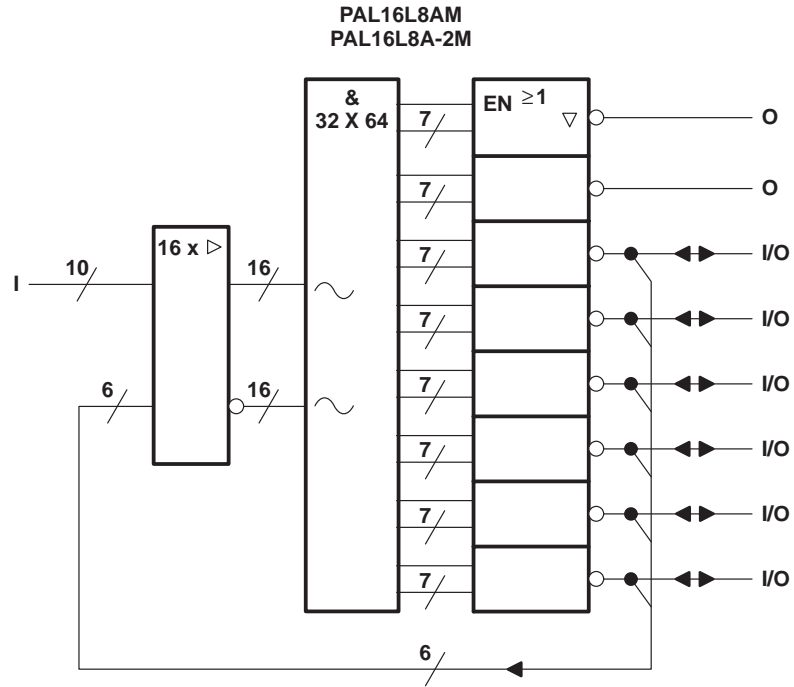
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PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M  
STANDARD HIGH-SPEED PAL® CIRCUITS

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functional block diagrams (positive logic)

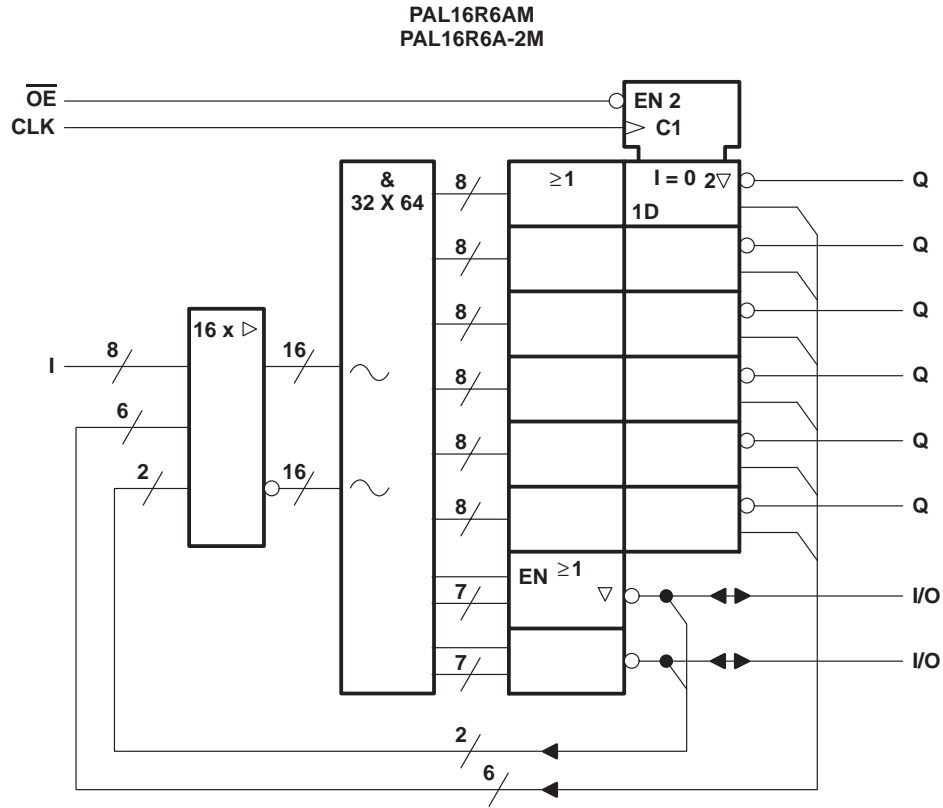


~ denotes fused inputs

# PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## functional block diagrams (positive logic)

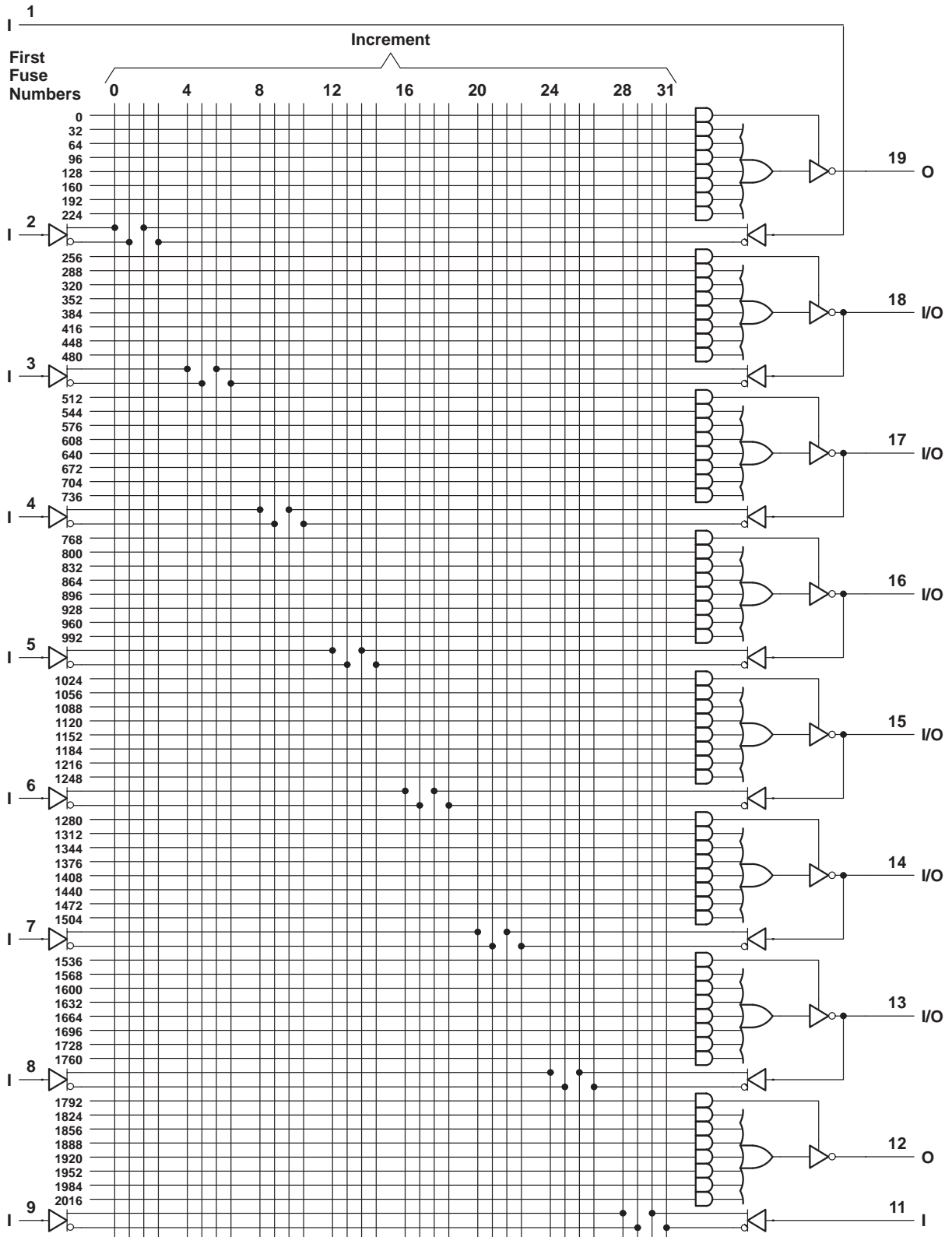


~ denotes fused inputs



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logic diagram (positive logic)

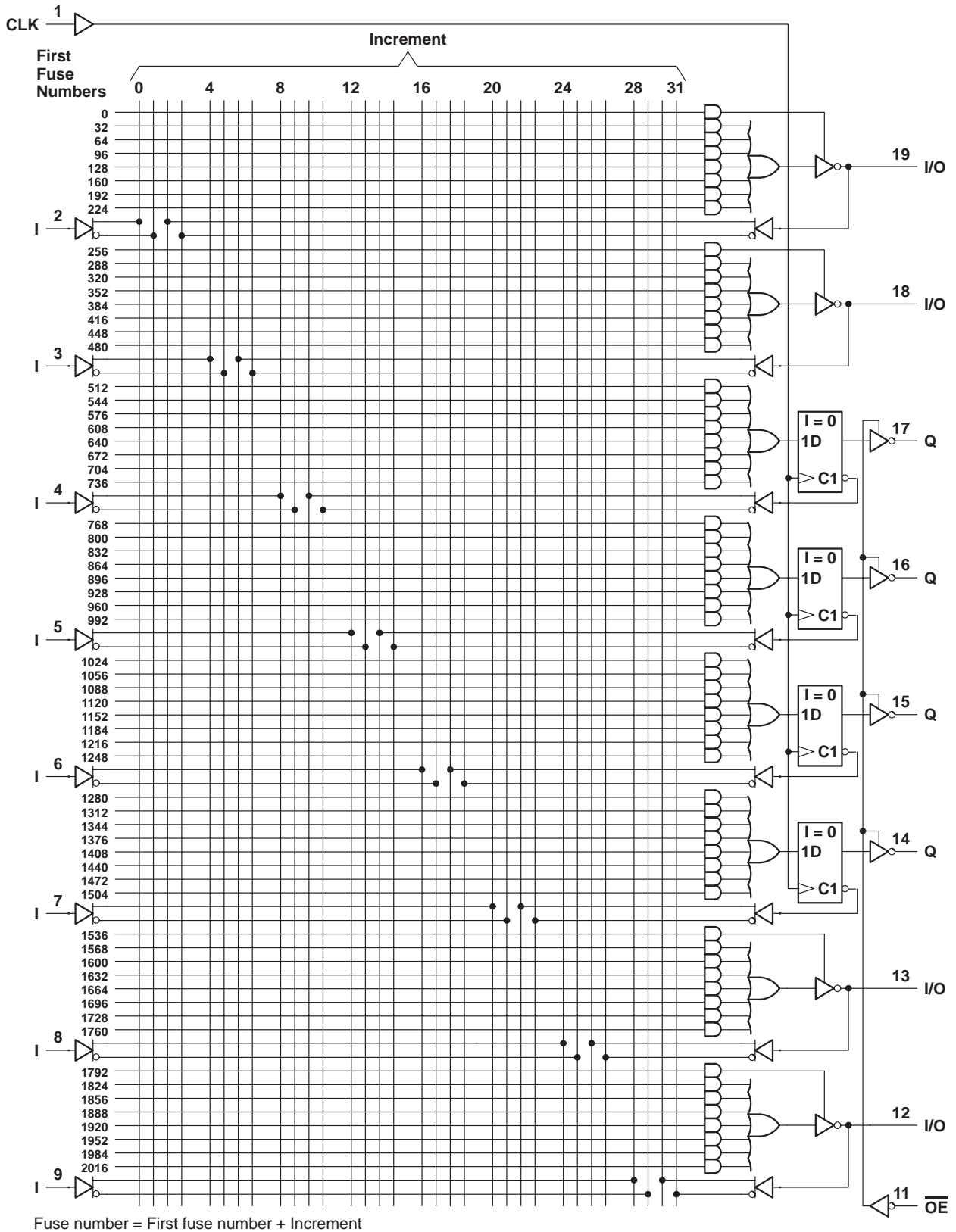


Fuse number = First fuse number + Increment

# PAL16R4AM, PAL16R4A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

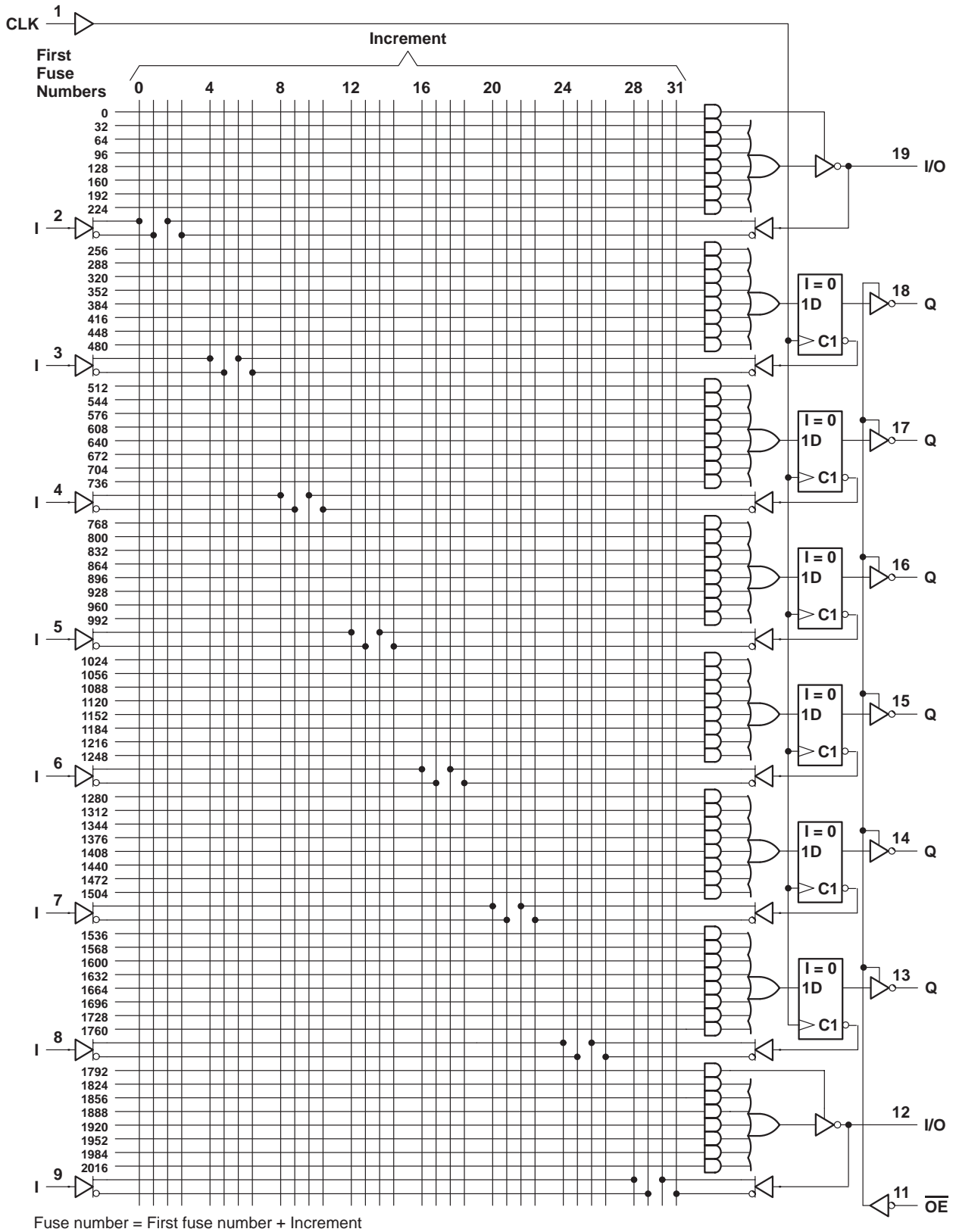
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## logic diagram (positive logic)



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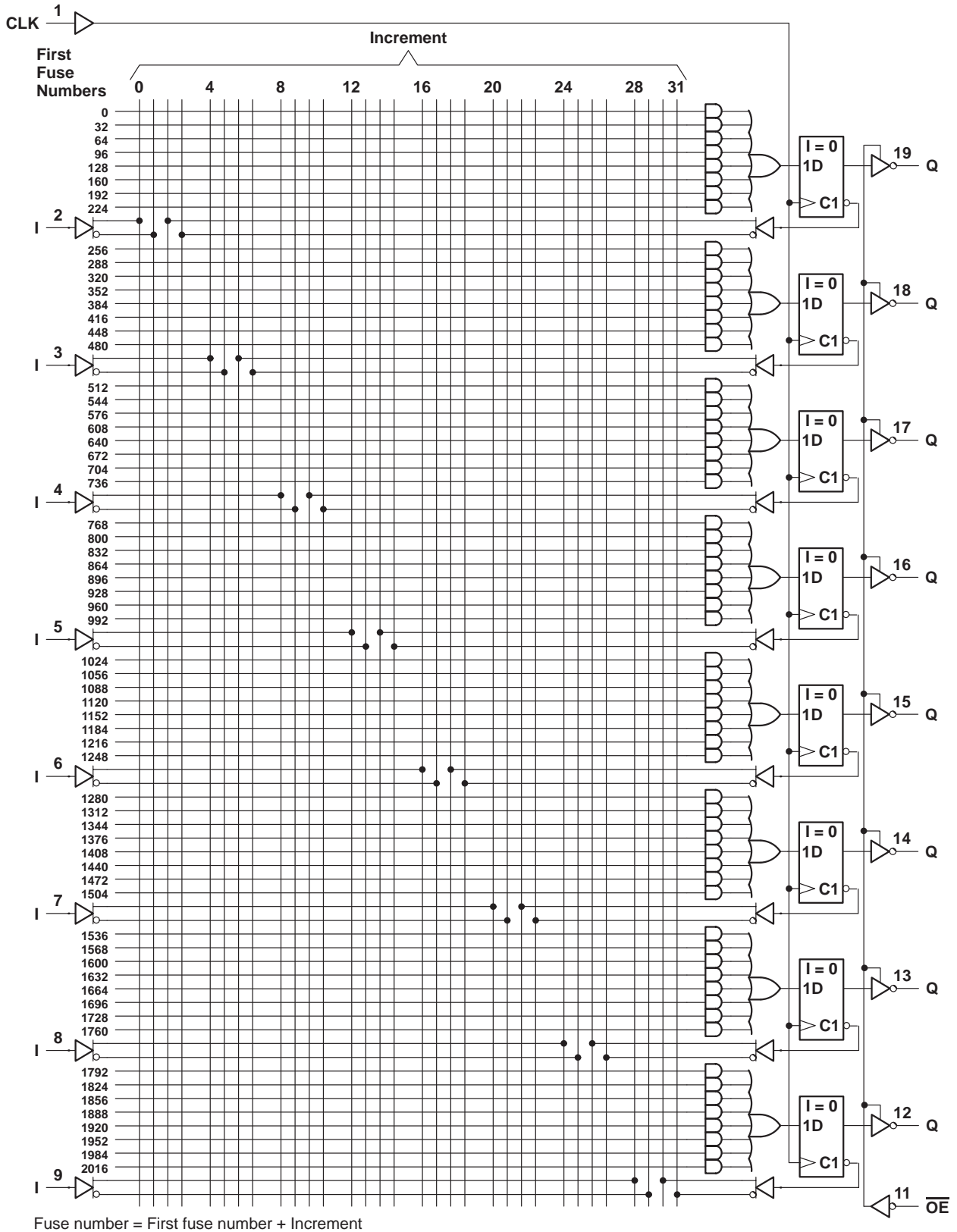
logic diagram (positive logic)



# PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## logic diagram (positive logic)



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**programming information**

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage (see Note 1) .....	5.5 V
Voltage applied to disabled output (see Note 1) .....	5.5 V
Operating free-air temperature range .....	–55°C to 125°C
Storage temperature range .....	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2		5.5	V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–2	mA
$I_{OL}$	Low-level output current			12	mA
$T_A$	Operating free-air temperature	–55	25	125	°C

# PAL16L8AM, PAL16R4AM, PAL16R6AM, PAL16R8AM STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.5	V	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -2 mA	2.4	3.2		V	
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA		0.25	0.4	V	
I <sub>OZH</sub>	Outputs	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20	μA	
	I/O ports					100		
I <sub>OZL</sub>	Outputs	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20	μA	
	I/O ports					-100		
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			0.2	mA	
I <sub>IH</sub>	I/O Ports	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			100	μA	
	All others					25		
I <sub>IL</sub>	$\overline{\text{OE}}$ input	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.2	mA	
	All others					-0.1		
I <sub>OS</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	-30		-250	mA	
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0, Outputs open			75	180	mA

## timing requirements

			MIN	MAX	UNIT
f <sub>clock</sub>	Clock Frequency		0	25	MHz
t <sub>w</sub>	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t <sub>su</sub>	Setup time, input or feedback before CLK↑		25		ns
t <sub>h</sub>	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f<sub>clock</sub>. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT	
f <sub>max</sub>			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	25	45		MHz	
t <sub>pd</sub>	I, I/O	O, I/O				15	30	ns
t <sub>pd</sub>	CLK↑	Q				10	20	ns
t <sub>en</sub>	$\overline{\text{OE}}$ ↓	Q				15	25	ns
t <sub>dis</sub>	$\overline{\text{OE}}$ ↑	Q				10	25	ns
t <sub>en</sub>	I, I/O	O, I/O				14	30	ns
t <sub>dis</sub>	I, I/O	O, I/O				13	30	ns

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V<sub>O</sub> at 0.5 V to avoid test equipment degradation.



# PAL16L8A-2M, PAL16R4A-2M, PAL16R6A-2M, PAL16R8A-2M STANDARD HIGH-SPEED PAL<sup>®</sup> CIRCUITS

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## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -2 mA	2.4	3.2		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA		0.25	0.4	V
I <sub>OZH</sub>	Outputs	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20	μA
	I/O ports					100	
I <sub>OZL</sub>	Outputs	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20	μA
	I/O ports					-100	
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			0.2	mA
I <sub>IH</sub>	I/O Ports	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			100	μA
	All others					25	
I <sub>IL</sub>	$\overline{\text{OE}}$ input	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.2	mA
	All others					-0.1	
I <sub>OS</sub> <sup>‡</sup>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	-30		-250	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0,      Outputs open		75	90	mA

## timing requirements

			MIN	MAX	UNIT
f <sub>clock</sub>	Clock Frequency		0	16	MHz
t <sub>w</sub>	Pulse duration (see Note 2)	Clock high	25		ns
		Clock low	25		
t <sub>su</sub>	Setup time, input or feedback before CLK <sup>↑</sup>		35		ns
t <sub>h</sub>	Hold time, input or feedback after CLK <sup>↑</sup>		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f<sub>clock</sub>. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

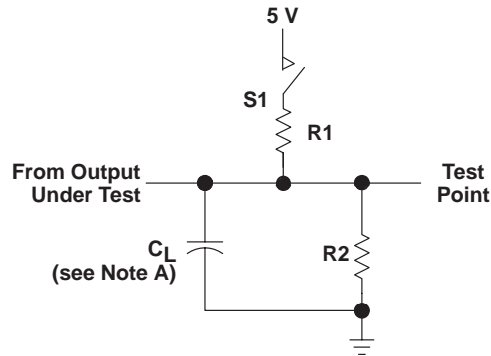
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP <sup>†</sup>	MAX	UNIT	
f <sub>max</sub>			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	16	25		MHz	
t <sub>pd</sub>	I, I/O	O, I/O				25	40	ns
t <sub>pd</sub>	CLK <sup>↑</sup>	Q			11	25		ns
t <sub>en</sub>	$\overline{\text{OE}}$ ↓	Q			20	25		ns
t <sub>dis</sub>	$\overline{\text{OE}}$ ↑	Q			11	25		ns
t <sub>en</sub>	I, I/O	O, I/O			25	40		ns
t <sub>dis</sub>	I, I/O	O, I/O			25	35		ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

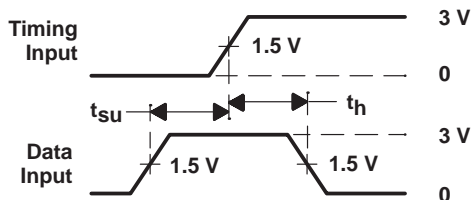
<sup>‡</sup> Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V<sub>O</sub> at 0.5 V to avoid test equipment degradation.



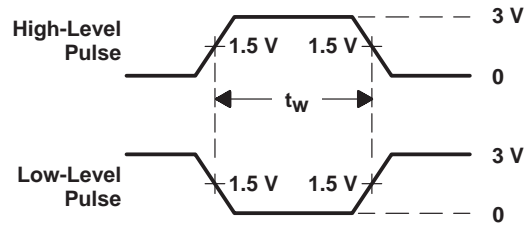
PARAMETER MEASUREMENT INFORMATION



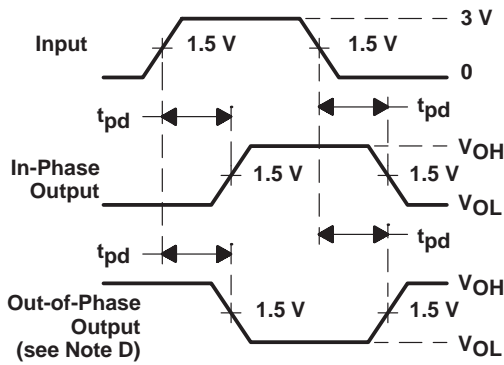
LOAD CIRCUIT FOR 3-STATE OUTPUTS



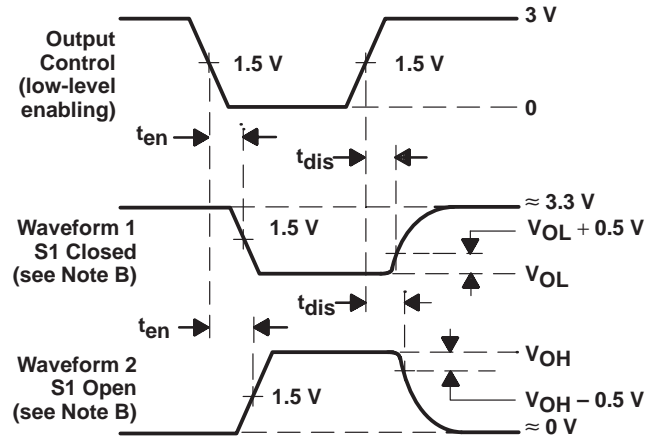
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATIONS



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics:  $PRR \leq 10$  MHz,  $t_r$  and  $t_f \leq 2$  ns, duty cycle = 50%  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
 E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

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