16-bits TCx

(Input, Output e Compare Units)

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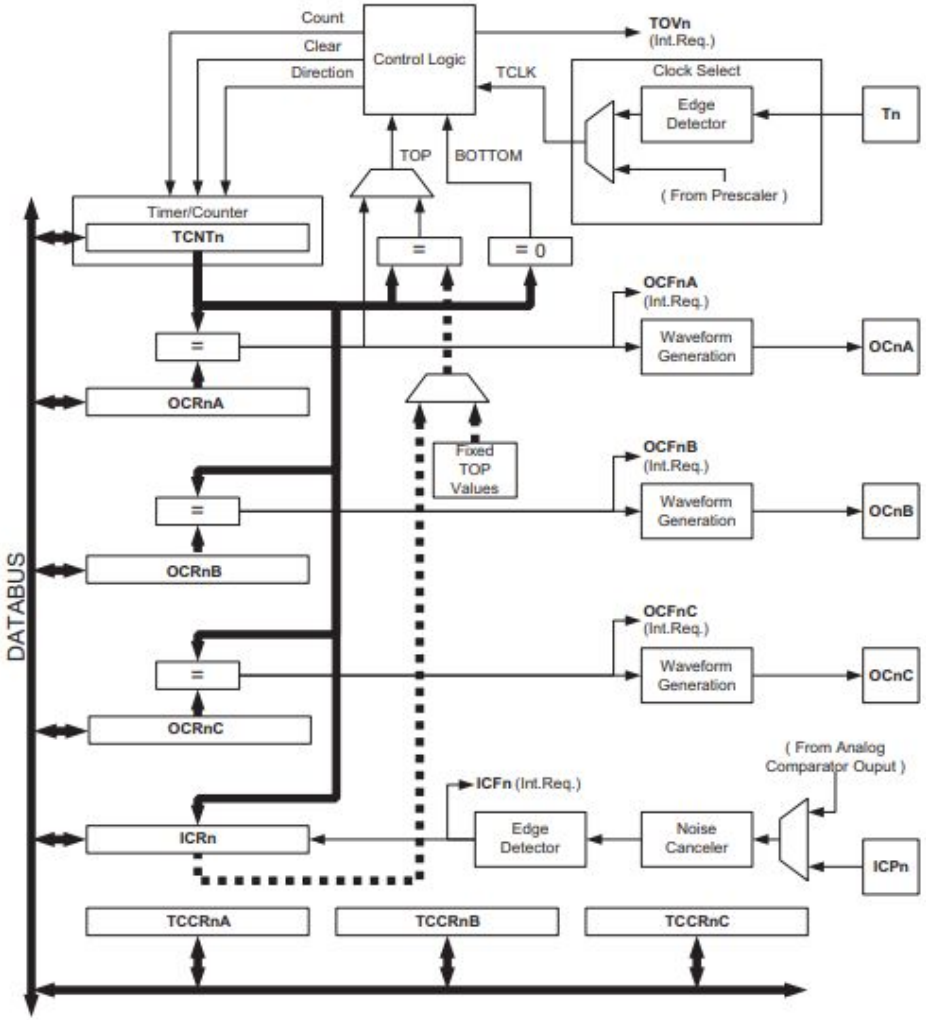
```
#include<avr/io.h>
#include<avr/interrupt.h>
#include<avr/delay.h>

#define LED PF0 // porta A0
#define BOTAO PD5 // porta T5

ISR (TIMER5_COMPA_vect)
{
    PORTF ^= (1 << LED);
    TCNT5 = 1;      // contador
}
```

```c
int main()
{
    DDRF = (0x01 << LED);   //Configure the PORTF0 as output
    DDRD = (0x00 << BOTAO); //Configure the PORTD0 as input

    PORTD = 0x00; //desabilita pull up interno

    TCNT5 = 1;

    OCR5A = 3;     // interrupção acontece depois de apertar 3 vezes o botão

    TCCR5A = 0x00; // Normal port operation
    TCCR5B = (1<<CS50) | (1<<CS51) | (1<<CS52);
    TIMSK5 = (1 << OCIE5A) ;
    sei();      // Enable global interrupts by setting global interrupt enable bit in SREG

    while(1)
    {

    }
}
```


Count
Clear
Direction
Control Logic
TOVn
(Int.Req.)
TCLK
Clock Select
Edge
Detector
Tn
(From Prescaler)
TOP
BOTTOM
Timer/Counter
TCNTn
=
= 0
OCFnA
(Int.Req.)
Waveform
Generation
OCnA
OCRnA
Fixed
TOP
Values
OCFnB
(Int.Req.)
OCnB
OCRnB
OCFnC
(Int.Req.)
OCnC
OCRnC
DATABUS
(From Analog
Comparator Ouput)
ICFn (Int.Req.)
ICRn
Edge
Detector
Noise
Canceler
ICPn
TCCRnA
TCCRnB
TCCRnC

Contador

TCNT5H and TCNT5L –Timer/Counter 5

Bit	7	6	5	4	3	2	1	0	
(0x125)	TCNT5[15:8]								TCNT5H
(0x124)	TCNT5[7:0]								TCNT5L
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Registrador de comparação

OCR5AH and OCR5AL – Output Compare Register 5 A

Bit	7	6	5	4	3	2	1	0	
(0x129)	OCR5A[15:8]								OCR5AH
(0x128)	OCR5A[7:0]								OCR5AL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TCCR5B – Timer/Counter 5 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0x121)	ICNC5	ICES5	–	WGM53	WGM52	CS52	CS51	CS50	TCCR5B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 17-6. Clock Select Bit Description

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}/1$ (No prescaling
0	1	0	$clk_{I/O}/8$ (From prescaler)
0	1	1	$clk_{I/O}/64$ (From prescaler)
1	0	0	$clk_{I/O}/256$ (From prescaler)
1	0	1	$clk_{I/O}/1024$ (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

Habilita interrupção

TIMSK5 – Timer/Counter 5 Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
(0x73)	–	–	ICIE5	–	OCIE5C	OCIE5B	OCIE5A	TOIE5	TIMSK5
Read/Write	R	R	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	